In re Patent Application of
DE SANTIS ET AL.
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In the Specification:

Please replace paragraph [00010] on page 3 with the following rewritten paragraphs:

~~On the basis of this solution idea the technical problem is solved by a sensing circuit as previously described and defined in the characterising part of claim 1.~~

In particular, the sensing circuit may comprise a first bias current generator connected between a first voltage reference and a first inner circuit node. At least one second reference current generator may be connected to the first reference voltage. A comparator may have a first input terminal connected to a comparison circuit node that is connected to the at least one second reference current generator, a second input terminal connected to a circuit node that is connected to the first inner circuit node, and at least one output terminal forming at least one output terminal of the sensing circuit.

A cascode-configured bias circuit may be connected between the inner circuit node and a matching circuit node. The cascode-configured bias circuit may also be connected to a second voltage reference. A current/voltage conversion stage may be connected to the matching circuit node, to the comparison circuit node, and to a third voltage reference. The cascode-configured bias circuit may comprise a first transistor connected between the inner circuit node and the matching circuit node, and an operational amplifier. The operational amplifier may have an output terminal connected to a control terminal of the first transistor, a first input terminal connected to the third voltage reference and a second

input terminal connected to the output terminal. The first transistor may comprise a P-channel MOS transistor.

The current/voltage conversion stage may comprise a second transistor that is diode-configured and is connected between the matching circuit node and the third voltage reference. A third transistor may be connected between the comparison circuit node and the third voltage reference. The third transistor comprises a control terminal that may be connected to the control terminal of the second transistor. The second and third transistors may comprise N-channel MOS transistors.

Another aspect of the present invention is directed to a memory device comprising at least one memory cell, and a sensing circuit as defined above connected thereto.

Yet another aspect of the present invention is directed to a method of making a sensing circuit as described above.